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EXAMINER	
TSAI, CAROL S W	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 01/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/898,674	MAWET, PATRICK H.	
	Examiner	Art Unit	
	Carol S Tsai	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,8-13,15-22,26-28,30 and 32-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19 and 36-45* is/are allowed.

6)☒ Claim(s) *1, 2, 4, 5, 8,15,20-22, 26, and 32* is/are rejected.

7)☒ Claim(s) *9-13,16-18,27,28,30 and 33-35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent No. 4,020,487 to Winter in view of U. S. Patent No. 5,459,427 to Chambers et al.

Winter discloses a signal processing system suitable for processing transducer signals in a low power measuring instrument (see col. 5, lines 5-12), the signal processing system comprising; a reference signal generator (ramp generator 20 shown on Fig. 1) for generating an ADC ramp signal (see col. 3, lines 41-43); two or more differential signal channels, each differential signal channel comprising: a first comparator (comparator 16 shown on Fig. 1) comprising a first input, a second input, and an output, the first input of the first comparator receiving the first signal of a pair of differential signals, the second input of the first comparator receiving the ramp signal, the output of the first comparator providing a first-comparator output signal based on the signals at the first and second inputs; and a second comparator (comparator 18 shown on Fig. 1) comprising a first input, a second input, and an output, the first input of the second comparator receiving the

second signal of the pair of differential signals, the second input of the second comparator receiving the ramp signal, the output of the second comparator providing a second-comparator output signal based on the signals at the first and second inputs (see Fig. 1 and col. 3, lines 37-58); and one or more digital differential value determining circuits (logic circuit 24 shown on Fig. 1) for receiving the first-comparator output signal and the second-comparator output signal of at least one of the differential signal channels and determining a digital value representative of the difference between the pair of differential signals received by the at least one differential signal channel; wherein the signal processing system is operable from a power supply to process the signals of the at least two differential signal channels in parallel and determine the corresponding digital values in parallel (see Fig. 1 and col. 7, lines 7-44).

Winter does not disclose a low voltage power supply providing voltage less than 1.75 volts.

Chambers et al. teach a low voltage power supply providing voltage less than 1.75 volts (see col. 3, line 60 to col. 4, line 4).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Winter's system to include the low voltage power supply providing a voltage less than 1.75 volts, as taught by Chambers et al., in order to permit the continued utilization of high performance analog signal processing functions for low power supply voltage applications (see Chambers et al. col. 4, lines 2-4).

As to claims 20-24, Winter also discloses a signal processing method suitable for processing transducer signals (see col. 5, lines 5-12) in a low power measuring instrument, the signal processing method comprising; generating an ADC ramp signal

(see col. 3, lines 41-43); for each of at least two differential signal channels; receiving the first signal of a pair of differential signals at a first input of a first comparator of the differential signal channel and receiving the ramp signal at a second input of the first comparator of the differential signal channel; outputting a first-comparator output signal based on the signals at the first and second inputs of the first comparator; and receiving the second signal of a pair of differential signals at a first input of a second comparator of the differential signal channel and receiving the ramp signal at a second input of the second comparator of the differential signal channel; outputting a second-comparator output signal based on the signals at the first and second inputs of the second comparator (see Fig. 1 and col. 3, lines 37-58); and determining a digital value representative of the difference between each pair of differential signals received by a differential signal channel based on the first-comparator output signal and the second-comparator output signal of that differential signal channel; wherein the generating, receiving, outputting and determining steps are performed to determine the digital values corresponding to each differential channel in parallel (see Fig. 1 and col. 7, lines 7-44).

Winter does not disclose generating, receiving, outputting and determining steps being performed using voltage signals which do not exceed 1.75 volts.

Chambers et al. teach generating, receiving, outputting and determining steps being performed using voltage signals which do not exceed 1.75 volts (see col. 3, line 60 to col. 4, line 4).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Winter's system to include generating, receiving, outputting and determining steps being performed using voltage signals which do not

exceed 1.75 volts, as taught by Chambers et al., in order to permit the continued utilization of high performance analog signal processing functions for low power supply voltage applications (see Chambers et al. col. 4, lines 2-4).

4. Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winter in view of Chambers et al. as applied to claim 1 above, and further in view of U. S. Patent No. 4,514,476 to Fitzgerald.

As noted above, with respect to claims 2 and 5, Winter in combination with Chambers et al. teach all the features of the claimed invention, but do not discloses low voltage power supply providing a voltage equal to or less than 1.5 volts.

Fitzgerald teaches a 1.5 volts button type battery providing a voltage equal to 1.5 volts (see col. 5, lines 52-59).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Winter in combination with Chambers et al.'s system to include low voltage power supply providing a voltage equal to or less than 1.5 volts, as taught by Fitzgerald, in order to provide sufficient electrical energy to power an measuring device.

5. Claims 4, 15, and 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Winter in view of Chambers et al. as applied to claims 1 and 20 above, and further in view of U.S. Patent No. 6,011,389 to Masreliez et al.

As noted above, Winter in combination with Chambers et al. teach all the features

of the claimed invention, but do not disclose portable low power supply supplying a total average current of 10 microamps or less to the portable measuring instrument during normal operation.

Masreliez et al. teach the portable low power supply supplying a total average current of 10 microamps or less to the portable measuring instrument during normal operation (see col. 22, lines 13-21).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Winter in combination with Chambers et al.'s system to include the portable low power supply supplying a total average current of 10 microamps or less to the portable measuring instrument during normal operation, as taught by Masreliez et al., in order that the driving circuit can be able to provide a low duty cycle, and provide a strong output signal from the receiver winding, while still using a very small average current and a rapid sampling rate (see Masreliez et al. col. 22, lines 23-27).

As to claims 15 and 32, Winter in combination with Chambers et al. do not disclose a low power measuring instrument operable to determine a measurement based on the digital values.

Masreliez et al. teach the low power measuring instrument operable to determine a measurement based on the digital values (see col. 11, lines 1-25).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Winter in combination with Chambers et al.'s system to include the low power measuring instrument operable to determine a measurement based on the digital values, as taught by Masreliez et al., in order that litter power can be

consumed to allow the transducer to be readily incorporated into hand-held, batter-powered measurement tools (see Masreliez et al. Abstract, lines 16-19).

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Winter in view of Chambers et al. as applied to claim 1 above, and further in view of U. S. Patent No. U. S. Patent No. 6,508,122 to McCall et al.

As noted above, Winter in combination with Chambers et al. teach all the features of the claimed invention, but do not disclose a circuit being fabricated on a single silicon substrate in an integrated circuit.

McCall et al. teach the circuit being fabricated on a single silicon substrate in an integrated circuit (see col. 2, lines 8-15 and col. 4, lines 25-31).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Winter in combination with Chambers et al. 's system to include the circuit being fabricated on a single silicon substrate in an integrated circuit, as taught by McCall et al., in order to obtain highly accurate, sensitive, stable angular rate measurements under dynamic environments (see McCall et al. col. 2, lines 12-14).

Allowable Subject Matter

7. Claims 9-13, 16-18, 27-30, and 33-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 19, 36, and 37-45 are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter:

U. S. Patent No. 4,020,487 to Winter is the reference closest to the claimed invention. Winter discloses a signal processing system suitable for processing transducer signals in a low power measuring instrument, the signal processing system comprising; a reference signal generator for generating an ADC ramp signal; one or more differential signal channels, each differential signal channel comprising: a first comparator comprising a first input, a second input, and an output, the first input of the first comparator receiving the first signal of a pair of differential signals, the second input of the first comparator receiving the ramp signal, the output of the first comparator providing a first-comparator output signal based on the signals at the first and second inputs; and a second comparator comprising a first input, a second input, and an output, the first input of the second comparator receiving the second signal of the pair of differential signals, the second input of the second comparator receiving the ramp signal, the output of the second comparator providing a second-comparator output signal based on the signals at the first and second inputs; and one or more digital differential value determining circuits for receiving the first-comparator output signal and the second-comparator output signal of at least one differential signal channel and determining a digital value representative of the difference between the pair of differential signals received by the at least one differential signal channel. However, Winter does not teach the one or more digital differential value determining circuits comprising at least one clock circuit configured such that for at least one comparator included in the clock circuit a trip-point voltage of the comparator and a voltage change rate of a clock ramp signal

input to the comparator being both controlled based on a common signal, such that variations in a voltage supplied to the clock during normal operation does not substantially affect the clock period; and including all of the other limitations in the respective independent claims.

Response to Arguments

10. Applicant's arguments filed 11/10/2003 have been fully considered but they are not persuasive.

Applicants argue that with regard to Chambers being utilized to modify Winter, according to applicant's understanding, the circuits of Chambers are applicable to DC level shifting of an analog signal, that to DC shift any of the ramp or differential input signals of Winter, or of applicant's disclosed invention (particularly starting with a power supply voltage of less than 1 .75 volts as now claimed in amended Claim 1) would needlessly introduce another potential error source into the critical signals, and would also reduce the available voltage swing of either the ramp signal or the differential input signals, in either case reducing the available analog signal-to-noise ratio and related accuracy of the circuits, that thus, applicant asserts that there is no teaching or suggestion, nor is there a motivation, to combine the circuit of Chambers with the circuits of Winter so as to achieve applicant's claimed invention. The Examiner disagrees with Applicants. It is well known in the art that a low voltage power supply can be stable and substantially immune to temperature variations, power supply variations, and noise. In addition, "Another object of the present invention is to provide a novel means for causing the reference signal applied to the comparators in an analog-to-digital converter of the single-

slope detection type to vary in the same manner as common mode noise voltages applied to the input terminals of the comparator. Still another object of the present is to provide a digital voltmeter of the single-slope detection type which has a low susceptibility to common mode noise voltage" and "a second input terminal for receiving a second input signal formed by the superposition of the common mode noise voltage on a second DC voltage, a ramp generator responsive to the second input signal and operative to separate the common mode noise voltage from the second input signal and to develop a ramp reference signal that is modulated by the common mode noise voltage, a first comparator having a first input connected to the first terminal for receiving the first input signal, a second input for receiving the modulated ramp reference signal, and a first output, the first comparator being responsive to the first input signal and the modulated ramp reference signal and operative to produce a first output signal on the first output which changes state when the voltage level of the modulated ramp reference signal exceeds the level of the first input signal" described respectively at col. 2, lines 25-34 and lines 36-46 of Winter also clearly indicate that noise is operative to be separated by the ramp generator ahead of comparator. As set forth in the art rejection, Winter discloses the claimed invention, except for a low voltage power supply providing a voltage less than 1.75 volts. Chambers et al. teach a low voltage power supply providing a voltage less than 1.75 volts (see col. 3, line 60 to col. 4, line 4) in order to permit the continued utilization of high performance analog signal processing functions for low power supply voltage applications (see Chambers et al. col. 4, lines 2-4). Therefore, the combination of Winter and Chambers et al. clearly teach the claimed invention. In addition, it is well

known in the art that a low voltage power supply can be stable and substantially immune to temperature variations, power supply variations, and noise.

Applicants argue that applicant asserts that it is not clear where the individual circuit techniques or elements of Chambers could somehow be substituted for the individual circuit techniques or elements of Winters, that Applicant further asserts that even if such a combination were somehow made, any resulting circuit would still include significantly more components than applicant's disclosed embodiments, including numerous resistors, which would contribute to significant power dissipation, and that in contrast, applicant discloses embodiments which include very few components and very few resistors, in order to enable applicant's claimed low voltage and low power operation, which applicant asserts is important when starting with a power supply voltage of less than 1 .75 volts, as now recited in amended Claim 1. The Examiner disagrees with Applicants. Applications having a low-voltage reference to operate at a relatively low power supply voltage, such as 3.3, 2.5, 1.8, 1.2 or less volts, in order to support most analog functions, for portable, battery-operated equipment or systems employing complex, high performance electronic circuitry having increased recently with the widespread use of cellular telephones, laptop computers, and other systems, is well known in the art. As set forth in the art rejection, Winter discloses the claimed invention, except for a low voltage power supply providing a voltage less than 1.75 volts. Chambers et al. teach a low voltage power supply providing a voltage less than 1.75 volts (see col. 3, line 60 to col. 4, line 4) in order to permit the continued utilization of high performance analog signal processing functions for low power supply voltage applications (see

Chambers et al. col. 4, lines 2-4). Therefore, the combination of Winter and Chambers et al. clearly teach the claimed invention.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carol S. Tsai whose telephone number is (703) 305-0851. The examiner can normally be reached on Monday-Friday from 7:30 AM to 4:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703) 308-1677. The fax number for TC 2800 is (703) 308-7382. Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the TC 2800 receptionist whose telephone number is (703) 308-1782.

In order to reduce pendency and avoid potential delays, Group 2800 is encouraging FAXing of responses to Office actions directly into the Group at (703) 308-7382. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2800 will be promptly forwarded to the examiner.

Carol S. W. Tsai

12/24/03